CLAIMS

WHAT IS CLAIMED:

1. A method of forming a substrate contact in a field effect transistor, comprising:

providing a substrate with an insulation layer formed thereon;

forming a semiconductor layer above the insulation layer;

forming a transistor in an active region of said semiconductor layer;

forming a first part of said substrate contact, said first part extending through said insulation layer and contacting said substrate, said first part having a first end that extends above a surface of said semiconductor layer; and

forming a second part of said substrate contact above said first part of said substrate contact, said second part being electrically coupled to said first end of said first part of said substrate contact.

2. The method of claim 1, further comprising:

depositing a dielectric layer stack comprising a stop layer in contact with a gate electrode of the field effect transistor;

thinning and planarizing the dielectric layer stack, wherein material of the dielectric layer stack is maintained over the gate electrode with a predefined thickness that insures coverage of the gate electrode;

forming a first substrate opening in the dielectric layer stack, the semiconductor layer, and the insulation layer by photolithography and etching;

filling the first substrate opening with a contact metal to form said first part;

removing excess contact metal from the dielectric layer stack to planarize the surface of the dielectric stack;

depositing a dielectric layer with a predefined thickness over the dielectric layer stack and the first substrate opening;

forming a second substrate contact opening over and aligned to the first part;

forming in the dielectric layer stack and the dielectric layer, by using the stop layer, a drain contact opening over the drain region, a source contact opening over the source region, and a gate contact opening over the gate electrode;

filling the second substrate contact opening with a second contact metal, thereby forming said second part; and

filling the drain contact opening, the source contact opening, and the gate contact opening with the second contact metal, thereby forming a drain contact, a source contact, and a gate contact.

3. The method of claim 2, wherein forming the second substrate contact opening, the drain contact opening, the source contact opening, and the gate contact opening is performed during the same etch process.

4. The method of claim 2, wherein filling the second substrate contact opening and filling the drain contact opening, the source contact opening, and the gate contact opening is performed during the same filling process.

5. The method of claim 2, wherein the dielectric layer stack is deposited by plasma enhanced chemical vapor deposition.

6. The method of claim 2, wherein the first substrate contact opening is formed so as to extend into the substrate.

7. The method of claim 2, wherein removing the excess contact metal comprises chemically mechanically polishing the surface so as to avoid any cavities formed therein.

8. The method of claim 2, wherein forming the second substrate contact opening, the drain contact opening, the source contact opening, and the gate contact opening is performed by simultaneously etching while the contact metal provides a high selectivity in removing material of the dielectric layer.

9. The method of claim 1, wherein forming the first part of the substrate contact and forming the second part of the substrate contact includes depositing a metal barrier layer prior to filling with the contact metal and the second contact metal, respectively.

10. The method of claim 2, wherein the contact metal and the second contact metal are the same.

11. The method of claim 2, wherein the dielectric layer comprises a material having a low dielectric constant k.

12. The method of claim 11, wherein the k is less than 4.0.

13. The method of claim 2, wherein the stop layer serves as an anti-reflecting coating.

14. The method of claim 13, wherein the stop layer comprises one of silicon nitride and silicon oxynitride.

15. The method of claim 2, wherein the material of the dielectric layer stack that is maintained over the gate electrode comprises material of the stop layer.